REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicant asserts that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1–3, 6–8, 10, 12, 19–23, 27, 28, 30, 32 and 39–54 are pending in the application.

Claims 1–3, 6–8, 10, 12, 19–23, 27, 28, 30, 32 and 39–54 have been rejected.

Claims 8, 10, 12, 27, 39 and 44 have been amended.

Applicant respectfully asserts that no new matter has been added.

Interview Summary

Applicants thank the Examiner for the courtesy of the Telephonic Interview with applicants' representatives on January 10, 2005.

In the Interview, as summarized in the Interview Summary dated January 10, 2005, the rejection of claims 1, 8, 19, 44, 45 and 51 was discussed. Regarding claim 44, Applicants' representatives asserted that Alidina et al. (US Patent No. 5987490) does not teach or fairly suggest that the tracing back of the states is performed in two clock cycles. Specifically, Applicants' representatives pointed out that Alidina et al. describes a device for determining the trace bits, and does not describe tracing back the states based on the trace bits, as discussed in the remarks below. Regarding claims 45 and 51, the Examiner believes that claims reciting the limitations of claims 45 and 51, would be allowable over the cited references. It was agreed the

Examiner will review Alidina et al., and will reconsider the rejections of claims 44, 45 and 51 in view of the remarks below. Regarding claim 8, it was agreed that amending claim 8 to include the term "simultaneously", would overcome the rejection of claim 8. It was also agreed the Examiner will reconsider the rejections of claims 1 and 19 in view of the remarks below. Applicants acknowledge that the agreements reached are subject to further searching as may be deemed necessary by the Examiner.

CLAIM REJECTIONS

Claim Rejections under 35 USC §102

Claims 8, 10, 12 and 44-54 were rejected under 35 USC §102(e) as being anticipated by Alidina et al.

Applicants respectfully traverse the rejection of claims 8, 10, 12 and 44-54 under 35 U.S.C. § 102(e), inter alia, because a prima facie case of anticipation has not been established, as discussed below.

As is well established, in order to successfully assert a prima facie case of anticipation, the Examiner must provide a single prior art document that teaches every element and limitation of the clam or claims being rejected.

Claims 8, 10 and 12

Claim 8 was amended to recite "at least three memory cell groups for storing in sequential order trace bits of at least three stages of Viterbi decoding of a binary convolution code, such that the trace bits of said at least three stages are simultaneously maintained by said storage device". As agreed in the interview of January 10, 2005, this language is not anticipated by Alidina et al. Specifically, Alidina et al. does not teach or fairly suggest storing in sequential

order trace bits of at least three stages of the Viterbi decoding, such that the trace bits of the at least three stages are simultaneously maintained.

Therefore, it is respectfully requested that the rejection of amended claim 8 under 35 USC §102(e) be withdrawn.

Furthermore, it is respectfully asserted that the distinguishing features of independent claim 8, as discussed above, would not have been obvious at the time the invention was made to a person skilled in the art, in view of Alidina et al., alone or in combination with any other cited references, including the Asano et al. reference discussed below in connection with claims 1-3, 6 and 7. Therefore, it is respectfully asserted that independent claim 8 is patentable, and thus allowable, over the prior art references on record.

Claim 10 has been amended in consistency with independent claim 8. Specifically, claim 10 has been amended to recite "at least one of said memory cell groups" instead of "said groups" for consistency.

Claim 12 has been amended to be dependent from claim 8.

Claim 10 and amended claim 12 are each directly dependent from independent claim 8 and incorporate all the elements of this claim. Therefore, it is respectfully submitted that claim 10 and amended claim 12 are patentable at least for the reasons set forth above.

Claims 44-54

Claim 44 has been amended to recite " based on sequentially stored trace bits of two or more of said stages".

When relating to claim 44, the Examiner contended that "Alidina discloses a method of tracing back bit by bit (stage by stage) states of binary convolution codes that are decoded using Viterbi decoding (abstract). Each clock cycle will trace back a number of bits."

Applicants strongly disagree with this statement. As explained in the interview of January 10, 2005, and in the instant application at page 4, line 1 – page 5, line 5, "for each source symbol received, there is a transition between states ... The trace bit associated with the transition is determined during the "select" step of the "add-compare-select" operation when calculating the weights." "... the trace bits are used to trace back the optimal path from a "final" state to an "original" state, the path and the original state enabling reconstruction of the transmitted data. ... one can wait until all of the transmitted symbols have been received in order to begin the traceback ... an alternative method is to begin the decoding procedure when the memory is full".

As pointed out by Applicants' representatives in the interview of January 10, 2005, the Viterbi algorithm includes two processes involving trace bits. The first process is to generate the trace bits as part of the output of the add-compare-select (ACS) operation. Indeed, each trace bit is an indication of which state was selected in the "select" portion of the add-compare-select operation. Alidina et al. describes "a dual-MAC processor optimized so that two Viterbi ACS operations, including traceback bit storage, can be executed in two machine cycles". The second process is to trace back the optimal path from a "final" state to an "original" state, the optimal path and the original state enabling reconstruction of the transmitted data.

While the abstract of Alidina et al. states that "two Viterbi ACS operations, including traceback bit storage, can be executed in two machine cycles", no mention is made whatsoever of the number of machine cycles required in the Viterbi traceback routine. **Indeed, Alidina et al. is silent as to any features of the Viterbi traceback routine,** other than to state "The third step is known as traceback. This step traces the maximum likelihood path through a trellis of

possible present state to next state transitions ... and reconstructs the path through the trellis to extract the original input data" (col. 2, lines 48 – 53).

Therefore, Applicants respectfully assert that Alidina et al. does not teach or fairly suggest, either expressly or inherently, "tracing back, stage by stage, in as few as two clock cycles per stage, states of binary convolution codes that are decoded using Viterbi decoding", as originally recited by claim 44.

Therefore, it is respectfully requested that the rejection of amended claim 44 under 35 USC §102(e) be withdrawn.

Furthermore, it is respectfully asserted that the distinguishing features of claim 44, as discussed above, would not have been obvious at the time the invention was made to a person skilled in the art, in view of Alidina et al., alone or in combination with any other cited references, including the Asano et al. reference discussed below in connection with claims 1-3, 6 and 7. Therefore, it is respectfully asserted that claim 44 is patentable, and thus allowable, over the prior art references on record.

Claim 45 is directly dependent from independent claim 44 and incorporates all the elements of this claim. Furthermore, Applicants respectfully assert that Alidina et al. does not teach or fairly suggest, either expressly or inherently "generating a generated B-bit binary representation having a least significant bit equal to a trace bit of a state of a particular stage and having (B-1) most significant bits equal to the (B-1) least significant bits of a B-bit binary representation of an index of said state ... wherein B is the logarithm to base 2 of the number of states in a stage", as recited by claim 45. Therefore, it is respectfully submitted that claim 45 is patentable at least for the reasons set forth above.

Claims 46-50 are each dependent, directly or indirectly, from claim 45 and incorporate all the elements of this claim. Therefore, it is respectfully submitted that claims 46-50 are patentable at least for the reasons set forth above.

Regarding claims 51-54, the Examiner contended that "Alidina discloses a method of tracing back bit by bit (stage by stage) states of binary convolution codes that are decoded using Viterbi decoding (abstract). Each clock cycle will trace back a number of bits. Alidina discloses the trace back bit is stored as the least significant bit then the data is left shifted when new data is available and this new trace back bit is stored."

Applicants strongly disagree with this statement, since Alidina et al. does not relate o the process of tracing back the states, as discussed above in relation with claim 44.

Claim 51 recites "generating a generated B-bit binary representation having a least significant bit equal to a trace bit of a state of a particular stage and having (B-1) most significant bits equal to the (B-1) least significant bits of a B-bit binary representation of an index of said state...wherein B is the integer part of the logarithm to base 2 of the number of states in a stage". Claim 54 recites "a memory element to store in its B least significant bits a B-bit binary representation of an index of a state of a stage, where B is the integer part of the logarithm to base 2 of the number of said states". Applicants respectfully assert that at least these features are not anticipated by Alidina et al.

Therefore, it is respectfully requested that the rejection of claims 51 and 54 under 35 USC §102(e) be withdrawn.

Furthermore, it is respectfully asserted that the distinguishing features of claims 51 and 54, as discussed above, would not have been obvious at the time the invention was made to a person skilled in the art, in view of Alidina et al., alone or in combination with any other cited

references, including the Asano et al. reference discussed below in connection with claims 1-3, 6 and 7. Therefore, it is respectfully asserted that claims 51 and 54 are patentable, and thus allowable, over the prior art references on record.

Claims 52 and 53 are each dependent, directly or indirectly, from claim 51 and incorporate all the elements of this claim. Therefore, it is respectfully submitted that claims 52 and 53 are patentable at least for the reasons set forth above.

Claim Rejections under 35 USC §103

Claims 19-23, 27, 28 and 39-43 were rejected under 35 USC §103(a) as being unpatentable over Alidina et al. Specifically, the Examiner contended that "it would have been obvious for one of ordinary skill in the art at the time of the invention to store the trace bits in sequential order in a first and second register rather than in the registers and an additional memory unit".

Applicants respectfully traverse the rejection of claims 19-23, 27, 28 and 39-43 under 35 USC §103(a) as being unpatentable over Alidina et al., inter alia, because a prima facie case of obviousness has not been established, as explained below.

Claim 19 recites "a first register and a second register to jointly store a single copy of trace bits of at least a portion of one stage" and "a storage device having memory cells, wherein for each of said multiple stages, a group of one or more memory cells is to store said trace bits in sequential order". The two registers 46 shown in FIG. 3 of Alidina at el. can store trace bits of at most two stages. Therefore, the two registers 46 of Alidina et al. may be considered to be "a first register and a second register to jointly store a single copy of trace bits of at least a portion of one stage", as recited by claim 19. However, the storage device recited by claim 19 is a separate

component of the binary convolution decoder, apart from the first register and second register, and able to store trace bits for each of the multiple stages. It is respectfully asserted that the distinguishing features of claim 19, as discussed above, would not have been obvious at the time the invention was made to a person skilled in the art, in view of Alidina et al., alone or in combination with any other cited references, including the Asano et al. reference discussed below in connection with claims 1-3, 6 and 7.

Claim 27 has been amended to include "the trace bits stored in said first and second registers". Amended claim 27 recites "saving in sequential order the trace bits stored in said first and second registers to a group of one or more memory cells".

Claim 39 has been amended to include "memory cells of a storage device such that the trace bits of at least three of said stages are simultaneously maintained by said storage device". Amended claim 39 recites "for each of said multiple stages, storing said trace bits in sequential order in a group of one or more memory cells of a storage device such that the trace bits of at least three of said stages are simultaneously maintained by said storage device". It is respectfully asserted that the distinguishing features of amended claims 27 and 39, as discussed above, would not have been obvious at the time the invention was made to a person skilled in the art, in view of Alidina et al., alone or in combination with any other cited references, including the Asano et al. reference discussed below in connection with claims 1-3, 6 and 7.

Therefore, it is respectfully requested that the rejection of claims 19, 27 and 39 under 35 USC §103(a) be withdrawn.

Claims 20-23 are each directly dependent from claim 19 and incorporate all the elements of this claim. Claim 28 is directly dependent from claim 27 and incorporates all the elements of this claim. Claims 40-43 are each directly dependent from claim 39 and incorporate all the

elements of this claim. Therefore, it is respectfully submitted that claims 20-23, 28 and 40-43 are patentable at least for the reasons set forth above.

Claims 1-3, 6 and 7

Claims 1–3, 6 and 7 were rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al. in view of Asano et al.

Applicants respectfully traverse the rejection of claims 1–3, 6 and 7 under 35 USC §103(a) as being unpatentable over Alidina et al. in view of Asano et al., inter alia, because a prima facie case of obviousness has not been established, as explained below.

As explained hereinabove with respect to the rejections under 35 USC 102, and as discussed in the interview of January 10, 2005, Alidina et al. discloses a dual-MAC processor to perform two Viterbi "add-compare-select" operations, including traceback bit storage, in two machine cycles (abstract). The processor includes two adders 32, each operating in split mode for the Viterbi operation: "The two adds are performed as 16-bit split adds in one of the two adders 32 ... the two subtracts are performed as 16-bit split subtracts on the other adder 32" (col. 8, lines 37 – 42). Signals 78 output from the adders 32 are stored in two registers 46 as trace bits generated by the "add-compare-select" operation (Fig. 3). Alidina et al. is silent as to the method or mechanism by which traceback is performed using the trace bits.

In contrast, Asano et al. discloses an arithmetic apparatus for performing the traceback using trace bits (called "path select signals" in Asano et al.) once the trace bits have already been calculated for several (or all) stages. Indeed, in FIGS. 3 – 6 of Asano et al, "data memory 1 stores ... path select signals". Therefore, the ALU 8 shown in FIGS. 3, 5 and 6 of Asano et al. does not operate "to determine trace bits for Viterbi decoding of a binary convolution code".

The Examiner's proposed modification of Alidina et al. to use a single ALU instead of two would destroy the intended function of Alidina et al., namely to perform two Viterbi "add-compare-select" operations in two machine cycles. Therefore, it is unlikely that a person of ordinary skill in the art would make such a modification.

Accordingly, Alidina et al. and Asano et al., alone or in combination, fail to teach or suggest all the limitations of claim 1.

Claims 2–3, 6 and 7 are each dependent, directly or indirectly, from claim 1 and include all the limitations of claim 1. Therefore, it is respectfully submitted that claims 2-3, 6 and 7 are patentable at least for the reasons set forth above.

Therefore, it is respectfully requested that the rejection of claims 1-3, 6 and 7 under 35 USC §103(a) be withdrawn.

CONCLUSION

The present communication is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested. It is submitted that the application is now in condition for allowance. Prompt notice of allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 05-0649.

Respectfully submitted,

Naim Shichrur
Agent for Applicants
Registration No. 56,248

Dated: January 18, 2005

Eitan, Pearl, Latzer & Cohen Zedek, LLP.
10 Rockefeller Plaza, Suite 1001
New York, New York 10020
Tel: (212) 632-3480
Fax: (212) 632-3490